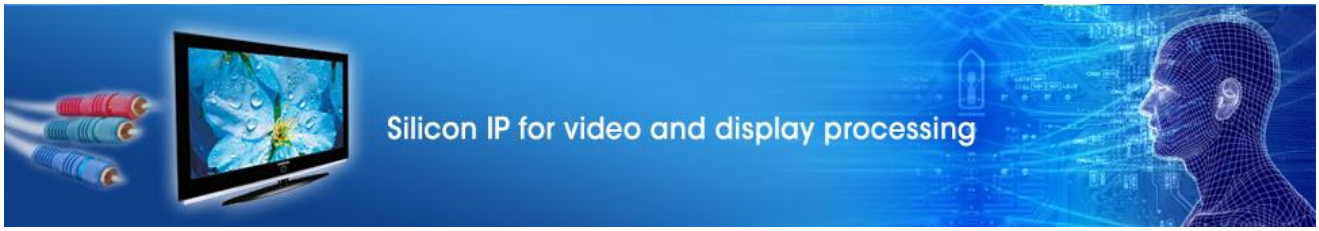

VSC-4KD Silicon IP Core

Video Scaler with Down Conversion from 4K

Overview

The VSC-4KD is a high quality polyphase scaler for down converting 4K inputs to standard definition or high definition format. 4K quadrant based format as used with Quad 3G-SDI links, as well as side-by-side format used with DisplayPort 1.2, are both supported. Pixels at the boundaries between tiles are processed correctly such that no seams are ever visible. The scaler may be used in conjunction with the VPC-1 Video Processor and Deinterlacer IP core or with any other customer or third party IP. Support for any scale factor allows full screen display of any input as well as arbitrary resizing for PIP and multiviewer applications. In addition, the core includes a number of Verilog parameters that allow it to be tailored at build time to satisfy specific requirements. Flexibility and robust design combine to make the VSC-4KD ideal for both consumer electronic and broadcast applications.

The VSC-4KD is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A VSC-4KD reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VSC-4KD IP core, the design also serves as a template for customer application development.

Features

- **General**
  - Any input <= 4096x2160p scaled to any output <= 2048x1080p
  - Supports both quadrant based format (Quad 3G-SDI) and side-by-side format (DisplayPort 1.2)
  - High quality polyphase scaling
  - Invisible seams between tiles
  - Dynamic resizing and aspect ratio conversion (ARC) without artifacts
  - Supports all frame rates up to 60 Hz
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
  - Seamless interface to VPC-1 deinterlacer
  - Fully synchronous design
- **Programmability**
  - Dynamically loadable coefficients for flexible image quality
  - Scale factors dynamically alterable without display artifacts
- **Build Time Options**
  - 4:2:2 or 4:4:4 data path
  - 8, 10 or 12-bit data path precision
  - Number of taps, number of phases, coefficient precision
  - Quadrant based or side-by-side format
- **Compatibility**
  - Use standalone or in conjunction with VPC-1 Video Processor and Deinterlacer
  - Support for both Xilinx and Altera devices

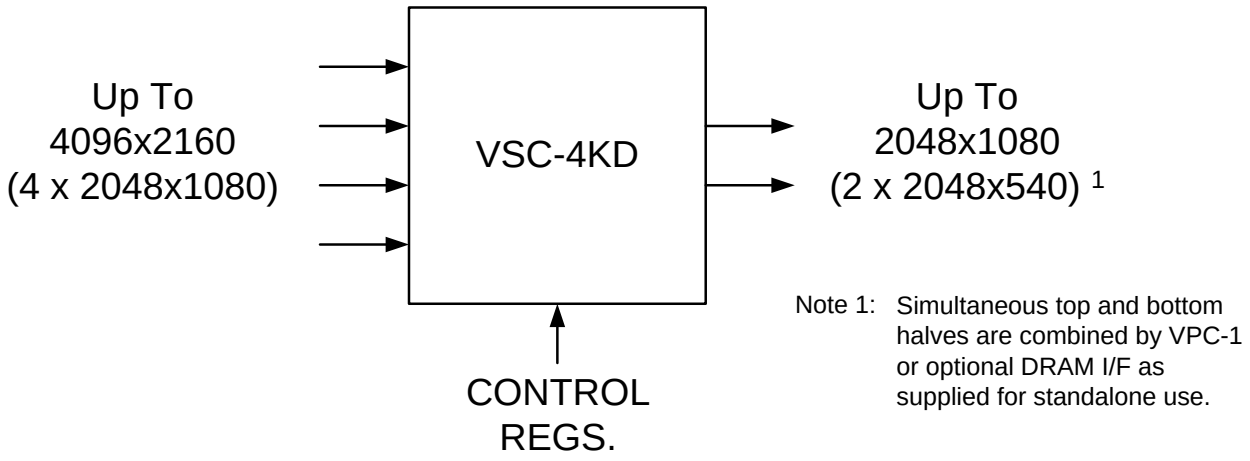

Fig.1 VSC-4KD (Quadrant Mode)

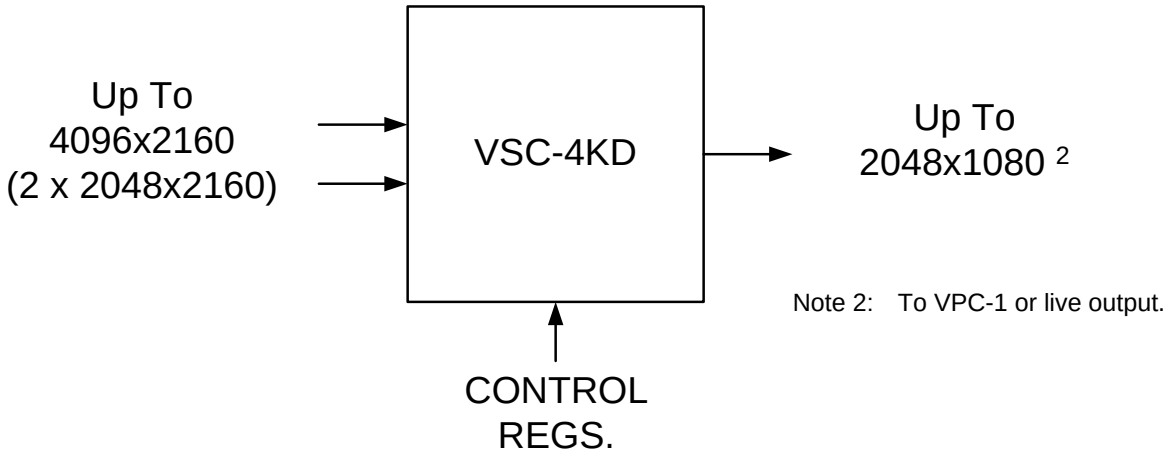

Fig.2 VSC-4KD (Side-by-Side Mode)

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support