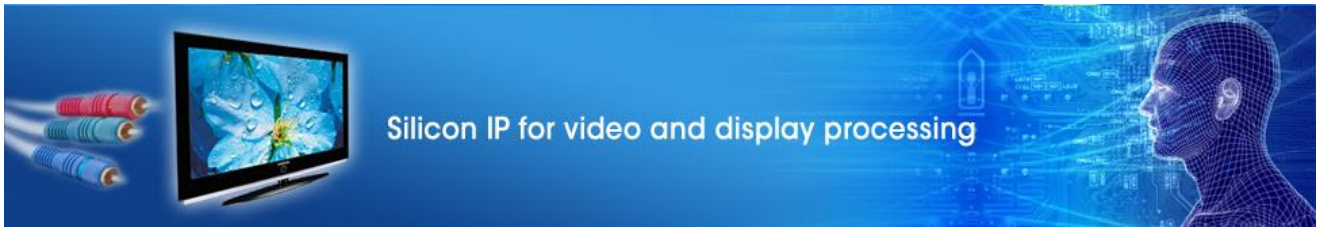

VPC-5 Silicon IP Core

Adaptive Detail Enhancer

Overview

The VPC-5 is a 2D adaptive detail enhancer which selectively enhances the appearance of edges and textures without enhancing the appearance of noise. Separate controls are provided for both edge and texture enhancement as well as for the amount of enhancement to be applied in each dimension. A programmable threshold for discriminating textures from noise is also provided. Careful algorithm design and piecewise linear control ensure a well behaved response without large changes at the output in response to small changes at the input. Programmable overshoot clamping is provided to limit the amount of overshoot associated with enhancement. The VPC-5 Adaptive Detail Enhancer can be combined with the VPC-3 Mosquito/Block Noise Reducer to provide a complete suite of enhancement and noise reduction tools.

The VPC-5 is available with complete Verilog source code, Verilog test bench and bit-accurate C model as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A VPC-5 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VPC-5 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - The following input formats are supported: 480p, 576p, 720p, 1080p and other custom formats (function should be located downstream from deinterlacer)
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
  - Low latency (~2 lines)
  - Fully synchronous design
- **Enhancement**
  - Selectively enhances sharpness of edges and textures
  - Separate controls provided for edge and texture enhancement
  - Enhances edges and textures without amplifying noise
  - Programmable threshold for discriminating textures from noise
  - Enhancement applied in both horizontal and vertical dimensions with separate level controls provided
  - Programmable overshoot clamping control
- **Compatibility**
  - Use standalone or in conjunction with other Crucial IP cores or third party IP
  - Support for both Xilinx and Altera devices

Edge/Texture Enhancement

Overshoot Clamping

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support