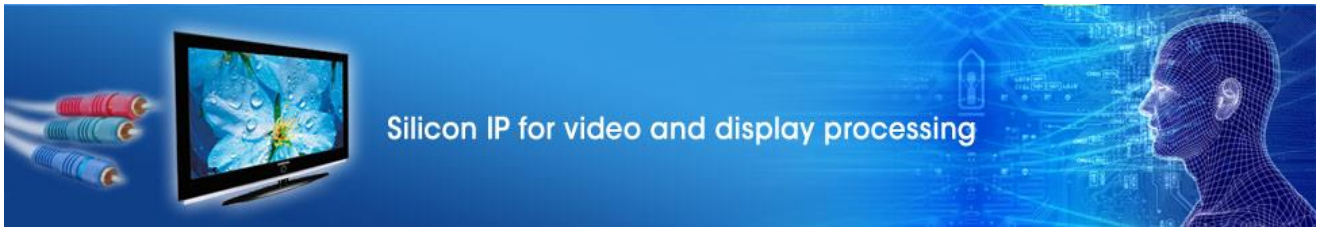


CMS-1 Silicon IP Core

Configurable Multi-Scaler

Overview

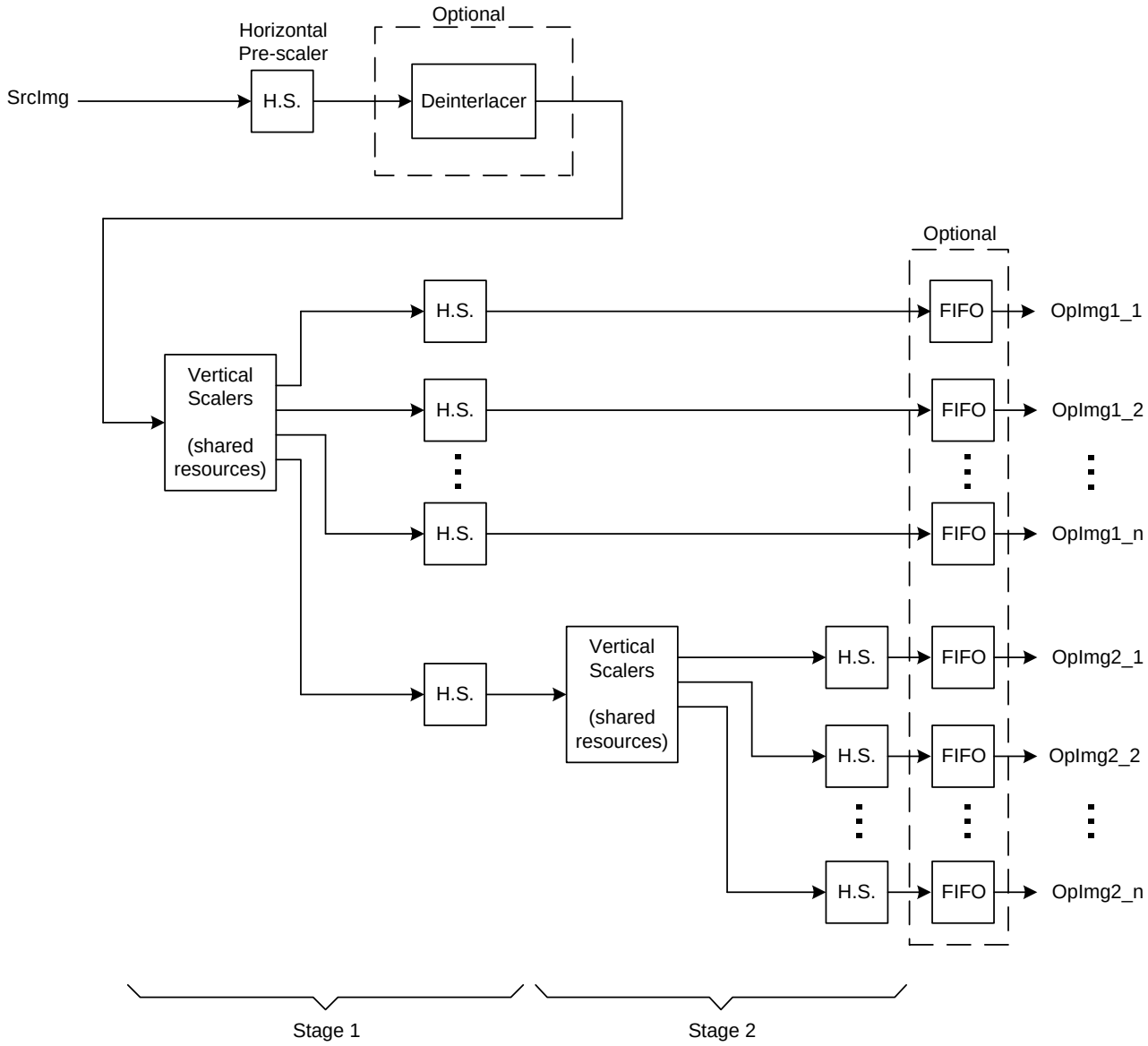
The CMS-1 is a parameterized integration of the VSC-1 scaler core with other IP as needed for ABR and similar applications requiring simultaneous multiple output formats from a single input. The CMS-1 is fully customizable through the use of Verilog parameters so that it may be tailored for use in various applications. The number of simultaneously available outputs, scaler taps, phases, data path and coefficient precision are all configurable. A highly efficient implementation exploits the use of cascading as well as resource sharing in order to minimize implementation cost. Flexible, high performance polyphase scaling based on the VSC-1 scaler core provides adequate filtering prior to down sampling to avoid aliasing artifacts. Optional deinterlacing is provided by the VPC-1 deinterlacer which can be included by setting a Verilog parameter (separate license required).

The CMS-1 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A CMS-1 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the CMS-1 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - Parameterized integration of VSC-1 scaler core with other IP to address ABR and similar applications requiring simultaneous multiple output formats from a single input
  - Highly efficient implementation exploits use of cascading and resource sharing
  - Input resolution up to 2K pixels with optional support for interlaced input
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
  - Optional output data smoothing buffers
- **Deinterlacing**
  - Optional high quality motion adaptive deinterlacing based on VPC-1 Deinterlacer IP core
- **Scaling**
  - High quality polyphase scaling based on VSC-1 Scaler IP core
  - Configurable number of taps, phases, data path and coefficient precision
- **Compatibility**
  - Support for both Xilinx and Altera devices



CMS-1 Block Diagram

Design Deliverables

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support